REMARKS

Claims 1-24 are pending in this application of which claims 1, 11, 19, and 20 are independent. Reconsideration in light of the following remarks is respectfully solicted.

Examiner's Interview

Examiner Tra and Primary Examiner Cunningham are thanked for their professionalism and courtesy during the Examiner's Interview of June 10, 2003. During the interview, the outstanding rejection to the claims under 35 USC 112 and 102 were discussed. The Examiners stated that the enablement rejection may be overcome with the submission of arguments on the record. These arguments can be found below.

Rejection of claims 1-24 under 35 U.S.C. § 112, first paragraph

The Examiner rejects claims 1-24 under 35 U.S.C. § 112, first paragraph, as being nonenabled. Specifically, the Examiner finds that newly added claim language ("independently of the voltage level of the first power supply" and "independently of the voltage level of the second power supply") is not supported by the specification. Applicants respectfully disagree.

"To be enabling, the specification...must teach those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation." (*See Durel Corp. V. Osram Sylvania Inc.*, 256 F.3d 1298 (Fed. Cir. 2001) (citing *Genenntech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997).) Moreover, routine experimentation does not constitute undue experimentation. (*See Johns Hopkins University v. Cellpro, Inc.*, 152 F.3d 1342 (Fed. Cir. 1998).)

In the present case, Fig. 1 illustrates two power-on detection circuits 10 and 11 for detecting power-on of the logic power supply VDDL and VDDH, respectively. The specification recites the following:

> The power-on detector 2 includes a power-on detection circuit 10 for detecting power-on of the logic power supply voltage VDDL and holding a power-on detection signal (power-on

> reset signal) /PORL at an active state while the logic power supply voltage VDDL is unstable (L level), a power-on detection circuit 11 coupled to receive the DRAM power supply voltage VDDH for holding, at the power-on of the DRAM power supply voltage VDDH, a power-on detection signal (power-on reset signal) /PORH at the active state (L level) until the power supply voltage VDDH becomes stable, and a main power-on detection circuit 12 responsive to these power-on detection signals /PORL and /PORH for maintaining a main power-on detection signal /POROH at the active state (L level) when at least one of the power-on detection signals is active. The main power-on detection signal /POROH from the main power-on detection circuit 12 is applied to the row decoder RD, the write driver WD and others in the DRAM macro DM. In other words, the main power-on detection signal /POROH is applied to a circuit part having the level conversion function.

(See Specification, page 9, 16-31).

The specification states that each of the power-on detection circuits detect power-on of the respective DRAM power supply voltage. There is no influence of power supply voltage VDDH on power-on detection circuit 10, and no influence of power supply voltage VDDL on power-on detection circuit 11. In other words, the power-on detection circuits 10 and 11 each detect VDDH and VDDL, respectively, without influence of the other power supply. This can be seen from Figs. 4 and 5 of the application. In these Figures, at power-on of VDDH, power-on detection circuit 10 outputs /PORH, which is fixed at the "L" level, until VDDH attains a stable state. At this time (Tb in Fig. 4), power-on detection circuit 10 outputs /PORH immediately rising to the "H" level. Similarly, at power-on of VDDL, power-on detection circuit 11 outputs a /PORL, which is fixed at the "L" level, until VDDL attains a stable state. At this time (Td in Fig. 4), power-on detection circuit 11 outputs /PORL immediately rising to the "H" level. At power-on of VDDL, there is no influence on the other power on detection circuit 10, as shown by a stable "H" level. Also, in Fig. 5, at power-on of VDDH, there is no influence on the other power-on detection circuit 11, as shown by the stable "H" level.

The illustrations of at least Figs. 1, 4, and 5, and associated text support the claim language "independently of the voltage level of the first power supply" and "independently of the voltage

level of the second power supply." Moreover, one of ordinary skill in the art would be able to make and use power-on detection circuits that operate independent of the voltage supplied to the other without undue experimentation, especially in light of the illustrations and timing diagrams of the specification. At the very least, simple routine extermination may be required. Accordingly, the enablement requirement has been satisfied. Withdrawal of the rejection is respectfully solicited.

Rejection of claims 1-24 under 35 U.S.C. § 112, second paragraph

The Examiner rejects claims 1-24 under 35 U.S.C. § 112, second paragraph, as being indefinite because the specification fails to disclose the detection circuits detecting first and second power supply voltages independently of another. Contrary to the requirements of § 112, second paragraph, the Examiner focuses on the specification, but does not address indefiniteness of claim language. It is believed that the Examiner should have made the rejection under the first paragraph, which addresses enablement of the specification. Nonetheless, the specification does indeed disclose the detection circuits detecting first and second power supply voltages independently of another. As discussed above, Figs. 4 and 5 illustrate such an operation. Withdrawal of the rejection is respectfully solicited.

Rejection of claims 1-3, 7, 19, 21 and 23 under 35 U.S.C. §102(e)

The Examiner maintains the rejection of claims 1-3, 7, 19, 21 and 23 under 35 U.S.C. §102(e) as being anticipated by Crotty. The rejection is respectfully traversed.

Noting the lack of enablement issue, the Examiner does not give any consideration to the detection circuits detecting "independently of the voltage level of the first power supply" and "independently of the voltage level of the second power supply," respectively. However, as the enablement issue has been aptly addressed, and presumably overcome, the Examiner is respectfully requested to consider these limitations. These limitations clearly distinguish the independent claims

from Crotty. More specifically, dual voltage detection circuit 210 of Crotty depends on both power supplies Vcc1 and Vcc2, *i.e.*, the power-on reset signal (VD1/POR1) obtains an active level when **both** of the power-on reset signals POR1, POR2 attain an active level. This is because Vcc2 drives the dual voltage detection circuit 210 for detecting Vcc1. Thus, Crotty does not teach detection circuits detecting "independently of the voltage level of the first power supply" and "independently of the voltage level of the second power supply," respectively, as the independent claims recite.

Furthermore, as to the "main power-on detection circuit," the Examiner takes the position that "active" [and "inactive"] are considered the states of a signal... a low state is seen as active state, and a high state is seen as inactive state." The Examiner takes this position because buffer circuit 650 (which the Examiner correlates is the claimed main power-on detection circuit) may be an AND gate, and asserts that the AND gate could output a main power-on detection signal in accordance with the claims. However, this interpretation is contrary to the operation of buffer circuit 650 disclosed by Crotty. On col. 9, lines 20-24, Crotty states that "[buffer] circuit 650 outputs a power-on reset signal POR, which is in the power-off logic level, if supply voltage Vcc1 is less than adequate **or** if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period time." Therefore, in order to employ an AND gate as the buffer, an active state of a Power-On Reset signal (POR1, POR2) must be a high state (and not a low state as asserted by the Examiner) to follow disclosed implementation of the buffer circuit 650. In other words, when any of the supply voltages are less than adequate, the POR signal must be in a power-off logic level, which corresponds to inputs to the AND gate of (0,0; 0,1; and 1,0). Buffer circuit outputs a power-on logic level (POR) when both (POR1 and POR2), and not one or the other (col. 9, lines 20-24), of the voltage supplies (Vcc1 and Vcc2) are adequate. To employ a power-on reset signal, rendered active from activation of a first activated power-on detection signal of the first and second power-on

detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals, would be contrary to the explicit teachings of Crotty.

In accordance with the foregoing, Crotty fails to identically disclose each and every element of independent claims 1, 11, 19, and 20. Claims dependent therefrom are patentable at least based on dependency to any one of these claims. Accordingly, the rejection of claims 1-3, 7, 19, 21 and 23 under 35 U.S.C. §102(e) as being anticipated by Crotty has been overcome. The rejection should be withdrawn.

Rejection of claims 11, 16-18, 20, 22, and 24 under 35 U.S.C. § 103(a)

The Examiner rejects of claims 11, 16-18, 20, 22, and 24 under 35 U.S.C. § 103(a) as being unpatentable over Crotty. In the Office Action of November 7, 2002, the Examiner acknowledged that Crotty does not disclose internal voltage generation circuits of 11 and 20, but asserts that it would have been obvious to use a voltage step-down circuit. On page 13 of the Amendment dated February 7, 2003, Applicants traversed and pointed out to the Examiner that a conclusion of obviousness must be factually supported, and evidence must be produced to support such a modification. In the current Office Action, and in response thereto, the Examiner simply states that "it is notorious well known in the art that a voltage step down circuit is [used]..." However, simply stating that something is "notoriously" well-known does not rise to the level of factual support of a modification. Applicants continue to seasonably traverse the Examiner's assertion that combination is notoriously well-known in the art. If notoriety is so high, the Examiner is requested to produce evidence thereof, as previously requested.

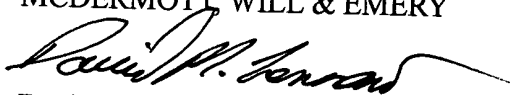
For the reasons discussed above and the reasons in connection with the anticipation rejection, Crotty fails to teach each and every element of claims 11 and 20. Moreover, the Examiner

has failed to establish a prima facie case of obviousness. Claims dependent therefrom are patentable at least based on dependency. Withdrawal of the rejection is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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